

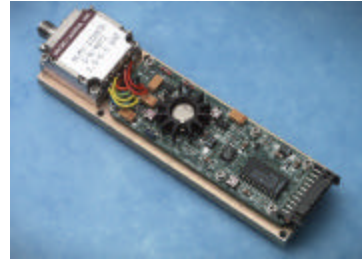


MICRO LAMBDA WIRELESS, INC.

MINIATURE YTO COMMERCIAL DIGITAL DRIVERS CD-SERIES

FEATURES

- 500 MHz to 8 GHz
- Compensation for Temperature Drift
- Voltage Regulators for Improved Stability
- 12 Bit Tuning Resolution
- Remote Oscillator/Driver Location



DESCRIPTION

Micro Lambda *MLMY Series* Miniature YIG Oscillators are available with integrated digital driver circuits. These drivers eliminate the need for customers to design or develop their own driver circuits and sophisticated test and alignment procedures. Integrating a driver at Micro Lambda's factory ensures peak performance. Alignment and compensation with the particular YIG oscillator can be maximized down to the component level.

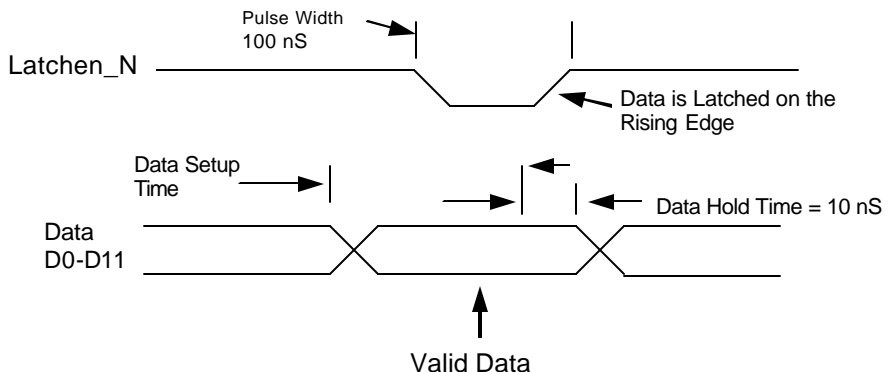
All drivers in this series provide input voltage regulators and compensation circuits to improve frequency drift. All voltages required by the YIG oscillator, except the heater inputs are supplied by the voltage regulators.

COMMERCIAL DIGITAL DRIVERS

.5- 8 GHz YTOs, CD & CG SERIES

DRIVER INPUT & RESPONSE	SPECIFICATION (0 to + 65 deg. C)
Tuning Command	Start Word (all 0's) = Lowest Frequency Stop Word (all 1's) = Highest Frequency
Tuning Resolution	12 BIT Positive Logic (Fmax-Fmin)/4095 Bit Resolution All Data Bits have internal 10k ohm pull-up resistors to +5V
Frequency Accuracy (excluding hysteresis)	See Table
Tuning Speed (Note 1)	5 mSec for 1 GHz step to within +/-10 MHz. (residual FM is 10 kHz Pk-Pk)
Main Driver Inputs	
Supply Voltage & Current	+15 V +/- .5 V @ 500 mA, Max. -15 V +/- .5 V @ 50 mA, Max.
Supply Voltage Pushing	+/- 100 kHz, Max. @ +/- .5 Vdc
Supply Voltage Ripple	10 mV Ripple Pk-Pk over 2 kHz to 3 MHz
Ground	Chassis Ground
YIG Heater Voltage & Current	+24 Vdc ±4 Vdc @ 300 mA surge for 2 seconds, 25 mA steady state Polarity independent : ±12 Vdc or ±15 Vdc acceptable
Latch Enable	LATCHEN_N is a TTL, 5V CMOS control line. It has an internal 10k-ohm pull-up resistor to +5 V. It is used to transfer the data on the bus to the digital driver circuit. TTL high = data ignored. Connect to Ground if enable is not required. If the unit is to be used on a computer data bus, the below timing Diagram applies. (All times = Minimum) 10 nS rise/fall latch transitions.

Note 1: Optional 1mS Tuning Speeds Available.



TIMING DIAGRAM

CD-SERIES — CONT.

FM Coil (CG Option)

Input Voltage	+/- 10V
Input Impedance	10 k Ohms
Sensitivity (Note 2)	+/- 2.5 MHz/V
Frequency Deviation	+/- 25 MHz

Note 2: FM Coil Sensitivity Adjustment Available. Sensitivity Stated is Average Over Frequency Range.

VXI/VME YIG Oscillators with Positive Input Digital Drivers (0° C to +65° C)

Model Number	Frequency GHz	Accuracy (MHz) *	Current +15 V (mA)	Current -15 V (mA)	Outline Drawing	Outline Drawing (CG-Option)
MLMY-0702CD	.7-2	+/- 5	200	50	81-069	**
MLMY-0204CD	2-4	+/- 6	300	100	81-069	**
MLMY-0306CD	3-6	+/- 9	400	100	81-069	**
MLMY-0408CD	4-8	+/- 12	500	100	81-069	**
MLMY-0206CD	2-6	+/- 9	400	100	81-069	**
MLMY-0208CD	2-8	+/- 12	500	100	81-069	**

* Accuracy includes frequency drift and linearity errors over the temperature range.

** Outline Drawing Available from Factory or Web-site.

Outline Drawing: 81-069

NOTE:
 1. WIRE GAUGE = 22-24 A.W.G.
 2. DATA - ALL OPS = Pass.
 ALL I/O = Pass.
 3. LATCH-EN 0 = DATA ACTIVE
 1 = DATA LATCHED

P1 - PIN CONNECTIONS

PIN NO	FUNCTION	PIN NO	FUNCTION
1	DATA BIT 0	11	DATA BIT 10
2	DATA BIT 1	12	DATA BIT 11 (MEMO)
3	DATA BIT 2	13	LATCHEN_N
4	DATA BIT 3	14	GND
5	DATA BIT 4	15	+ SUPPLY
6	DATA BIT 5	16	- SUPPLY
7	DATA BIT 6	17	FEATER (+ V)
8	DATA BIT 7	18	FEATER (GND)
9	DATA BIT 8	19	FM +
10	DATA BIT 9	20	FM -

REV | **DESCRIPTION** | **DATE** | **APPROVED**

UNLESS OTHERWISE SPECIFIED
 DIMENSIONS ARE IN INCHES
 TOLERANCES ARE:
 FRACTIONS DECIMALS ANGLES
 .0000 .0000 .0000

WEIGHT: 4 Oz.

CONTRACT NO. | APPROVALS | DATE

DESIGNER: HUNGMEN | DATE: 6/19/96

CHECKED: DS | DATE: 6/19/96

ISSUED: | DATE: ORN63 | P.W. NO.: 81-069

MICRO LAMBDA, INC.
 MINI OSC. W/DIGITAL DRV. (OPEN BOARD)

SCALE: 1:1