MICRO LAMBDA WIRELESS, INC.

1.0 INCH CUBE YTO
COMMERCIAL SERIAL DRIVERS
SD-SERIES

FEATURES
- 700 MHz To 18 GHz
- Compensation for Temperature Drift
- Voltage Regulators for Improved Stability
- 16 Bit Tuning Resolution

APPLICATIONS
Frequency Converters
Portable Test Equipment

DESCRIPTION

Micro Lambda ***MLOM and MLXM Series*** 1" Cube YIG Oscillators are available with integrated serial driver circuits. These drivers eliminate the need for customers to design or develop their own driver circuits and sophisticated test and alignment procedures. Integrating a driver at Micro Lambda's factory ensures peak performance. Alignment and compensation with the particular YIG oscillator can be maximized down to the component level.

All drivers in this series provide input voltage regulators, reverse voltage/ dataline protection and compensation circuits to improve frequency drift. All voltages required by the YIG oscillator, except the heater inputs are supplied by the voltage regulators.

COMMERCIAL SERIAL DRIVERS	**.7-18 GHz YTOs, SD & SG SERIES**
DRIVER INPUT & RESPONSE	SPECIFICATION (0 to +65 deg. C)
Tuning Command	Start Word (all 0's) = Lowest Frequency Stop Word (all 1's) = Highest Frequency
Tuning Resolution	16 BIT Positive Logic (Fmax-Fmin)/65,535 Bit Resolution
Tuning Accuracy (excluding hysteresis)	See Table
Tuning Speed	5 mS for 1 GHz step to within ±10 MHz. (residual FM is 10 kHz Pk-Pk)
Main Driver Inputs	
Supply Voltage & Current	+15 V ± .5 V @ Oscillator Tuning Current +50 mA, Max. -15 V ± .5 V @ 50 mA, (Plus Oscillator –5 Vdc Current if any) Max.
Supply Voltage Pushing	± 100 kHz, Max. @ ± .5 Vdc
Supply Voltage Ripple	10 mV Ripple Pk-Pk over 2 kHz to 3 MHz
Ground	Chassis Ground
YIG Heater Voltage & Current	+24 Vdc ±4 Vdc @ 300 mA surge for 2 seconds, 25 mA steady state Polarity independent : ±12 Vdc or ±15 Vdc acceptable
Digital Interface	The MLWI digital driver interface is a standard 3-wire connection compatable with SPI/QSPI/MICROWIRE interfaces. The chip-select input (CSELECTn) frames the serial data loading at the data input pin (DATA). Immediately following CSELECTn's high-to-low transition, the data is shifted synchronously and latched into the input register on the rising edge of the serial-clock input (CLOCK). After 16 data bits have been loaded into the serial input register, it transfers its contents to the DAC latch on CSELECTn's low-to-high transition (Figure 2). Note that if CSELECTn does not remain low during the entire 16 CLOCK cycles, data will be corrupted. In this case, reload the DAC latch with a new 16-bit word.

Micro Lambda Wireless, Inc. - 46515 Landing Parkway, Fremont California 94538 * Phone (510) 770-9221 * Fax (510) 770-9213

Power-On Reset

The MLWI digital driver has a power-on reset circuit to set the DAC’s output to OV(F-min) in unipolar mode when VDD is first applied. This ensures that unwanted DAC output voltages will not occur immediately following a system power-up, such as after power loss.

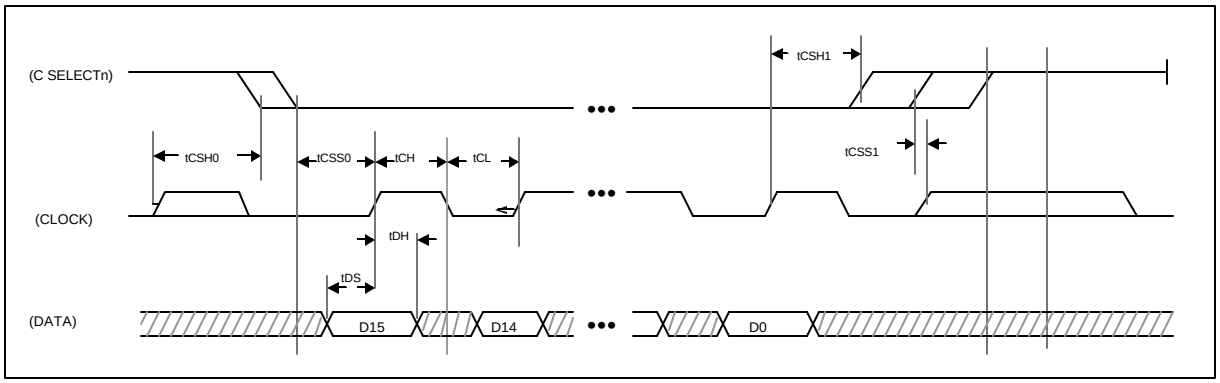


Figure 1. Timing Diagram

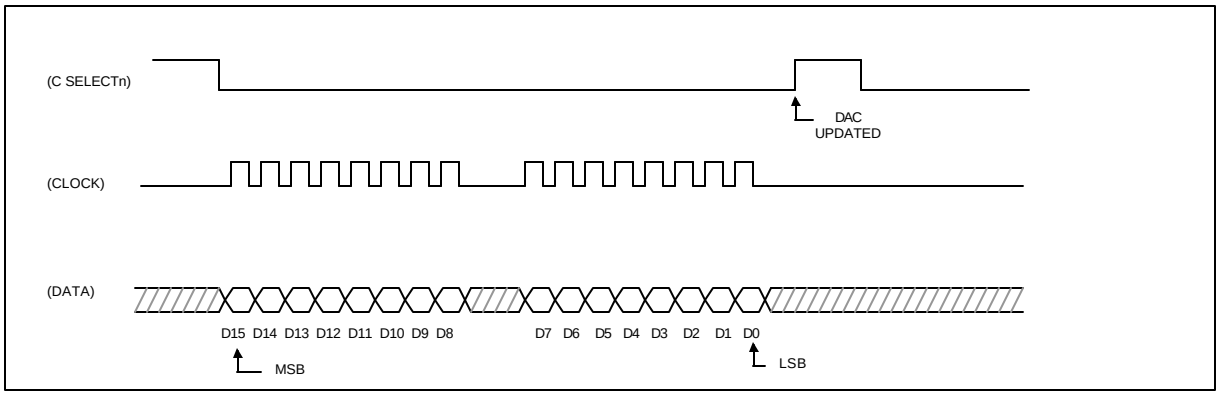


Figure 2. 3-Wire Interface Timing Diagram

TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK Frequency	fCLK				10	MHz
CLOCK Pulse Width High	tCH		45			ns
CLOCK Pulse Width Low	tCL		45			ns
CSn Low to CLOCK High Setup	tCSS0		45			ns
CSn High to CLOCK High Setup	tCSS1		45			ns
CLOCK High to CSn Low Hold	tCSH0		30			ns
CLOCK High to CSn High Hold	tCSH1		45			ns
DATA to CLOCK High Setup	tDS		40			ns
DATA to CLOCK High Hold	tDH		0			ns
VDD High to CSn Low (power-up delay)				20		µs

FM Coil Driver (SG Option)

Voltage	± 10 V
Current	± 100 mA
Input Impedance	1 k-Ohms
Sensitivity (Note 1)	± 2.5 MHz/V
Frequency Deviation	± 25 MHz

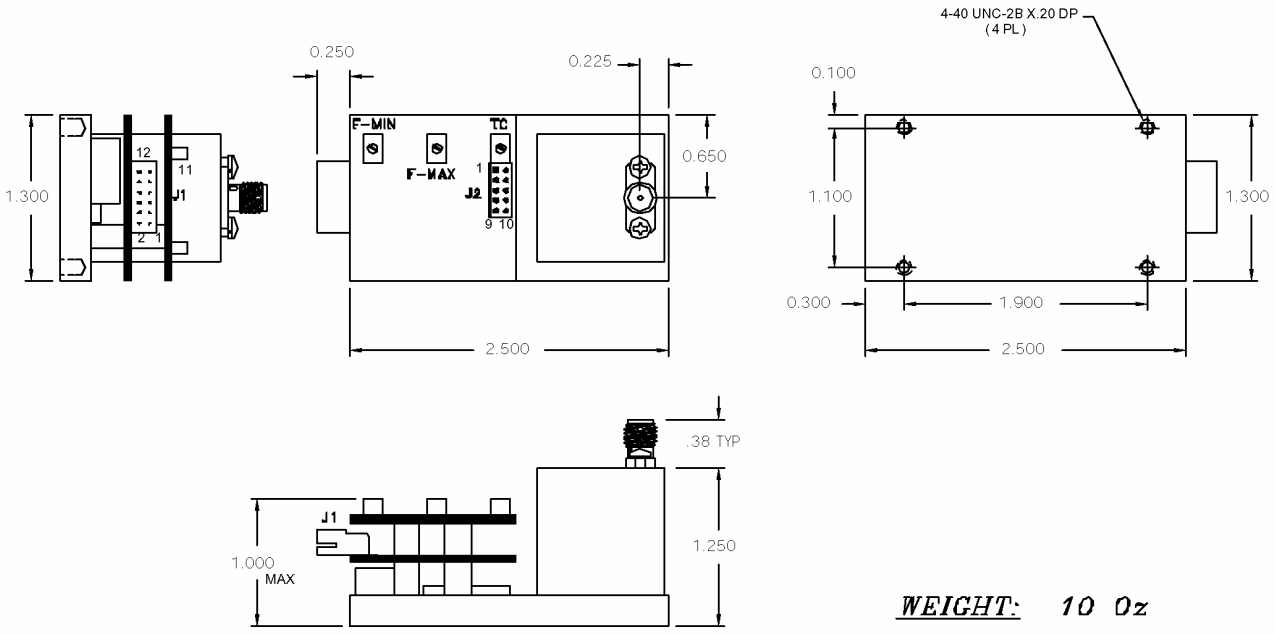
Note: 1. FM Coil Sensitivity Adjustment Available. Sensitivity Stated is Average Over Frequency Range.

PERFORMANCE SPECIFICATIONS

1.0" Cube YIG Oscillator with Serial Drivers (0° C to +65° C)

Model Number	Frequency GHz	Accuracy (MHz) *	Current +15 V (mA)	Current -15 V (mA)	Outline Drawing	Outline Drawing (SG Option)
Octave Bands						
MLOM-0102SD	1-2	± 3	200	50	11-112	**
MLOM-0204SD	2-4	± 6	300	50	11-112	**
MLOM-0408SD	4-8	± 8	500	50	11-112	**
MLOM-0812SD	8-12.4	± 12	700	50	11-112	**
MLOM-1218SD	12-18	± 14	1100	50	11-112	**
Multi-Octave Bands						
MLOM-0702SD	.7-2	± 3	200	50	11-112	**
MLOM-0704SD	.7-4	± 5	300	50	11-112	**
MLOM-0208SD	2-8	± 12	500	50	11-112	**
MLOM-0306SD	3-6	± 8	400	50	11-112	**
MLOM-0210SD	2-10	± 15	600	100	11-112	**
MLOM-0310SD	3.5-10.5	± 15	600	100	11-112	**
MLOM-0412SD	4-12.4	± 16	700	100	11-112	**
MLOM-0716SD	7-16	± 18	900	50	11-112	**
MLOM-0818SD	8-18	± 18	1100	50	11-112	**
MLXM-0818SD	8-18	± 18	1225	100	11-112	**

* Accuracy includes frequency drift and linearity errors over the temperature range.
** Outline Drawing Available from Factory or Web-site.



WEIGHT: *10 Oz*

BOTTOM BOARD (DAC BOARD)
J1 (2MM DUAL ROW TERMINAL STRIP)

DIGIKEY PART # : H2065-ND
MATING WITH # : H2141-ND

PIN	*FUNCTIONS*	
1	CLOCK	
2	DATA	
3	CSELECTn	
4	GROUND	
5	-V SUPPLY	
6	+V SUPPLY	
7	HEATER 1	
8	HEATER 2	
9	FM +	(*)
10	FM -	(*)
11	N/C	
12	N/C	

NOTES:

1- (*) : NOT USED FOR FILTER

2- RECOMMENDED WIRE SIZE = 20-22 GAUGE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ARE : FRACTIONS ± DECIMALS XX ± .010 XXX ± .005 ANGLES ±	CONTRACT NO.	MICRO LAMBDA WIRELESS, INC.	
MATERIAL	APPROVALS / DATE DRAWN N.NGUYEN 4/11/02 CHECKED	*1" OSC. W/ 1.3" 16 BIT SERIAL DIGITAL DRIVER*	
FINISH	ISSUED	SIZE	CAGE No. ORN63 / DWG NO. 11 - 112 / REV. A
DO NOT SCALE DRAWING			